Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

In the Claims:

1. (Currently amended) A phase-lock loop comprising:

an oscillator having an output oscillator signal whose frequency is related to a received error-correction signal:

a phase-frequency circuit~~detector~~ receiving the oscillator signal and a reference signal and generating at a controllable rate ~~the~~ error-correction pulses~~signal~~ based on ~~the~~ a phase difference between~~of~~ the oscillator signal and the reference signal;

a filter generating the error-correction signal ~~connecting the error correction signal~~ from the error-correction pulses~~phase-frequency detector to the oscillator~~, the filter including a capacitor; and

a rate selector coupled to the capacitor and to the phase-frequency circuit, monitoring a charge on the capacitor, and controlling the rate at which the phase-frequency circuit generates ~~of~~ the error-corr~~n~~nection pulses~~signals~~ to equal any one of more than two rates as a function of the charge on the capacitor.

2. (Currently amended) The phase-lock loop according to Claim 1, wherein:

the phase-detector circuit determines the phase difference between the oscillator and reference signals during phase-comparison cycles; and

the rate selector sets the rate of the error-connection pulses~~signals~~ to once per each of the comparison cycles ~~of the phase-frequency detector~~ until the charge ~~reaches~~ equals a first threshold value, and decreases the rate to less than once per each of the comparison cycles after the charge ~~has~~ equals~~reached~~ the first threshold value.

3. (Currently amended) The phase-lock loop according to Claim 2, wherein the rate selector detects a plurality of increasing threshold values of charge on the capacitor and, in response to the increasing threshold values of charge, causes the phase-frequency circuit to generate ~~controls~~ the ~~variable rate~~ error-correction pulses ~~to a corresponding~~ at respective ~~plurality of~~ decreasing rates.

4. (Currently amended) A phase-lock loop comprising:

an oscillator having an output oscillator signal whose frequency is related to a received error-correction signal:

a phase-frequency circuit receiving the oscillator signal and a reference signal and generating at a controllable rate the error-correction pulses based on the a phase difference between the oscillator signal and the reference signal;

a filter generating the error-correction signal from the error-correction pulses, the filter including a capacitor;

a rate selector coupled to the capacitor and to the phase-frequency circuit, monitoring a charge on the capacitor, and controlling the rate at which the phase-frequency circuit generates of the error-correction pulses as a function of the charge on the capacitor;

wherein the phase-detector circuit determines the phase difference between the oscillator and reference signals during phase-comparison cycles;

wherein the rate selector sets the rate of the error-connection pulses to once per each of the comparison cycles until the charge equals a first threshold value, and decreases the rate to less than once per each of the comparison cycles after the charge equals the first threshold value;~~The phase-lock loop according to Claim 2,~~

wherein the rate selector includes a cycle counter to count the comparison cycles; and

wherein the rate selector uses the counter to set the decreasing ~~variable~~ rates of the error-correction pulses.

5. (Currently amended) The phase-lock loop according to Claim 2,

wherein the rate selector sets the rate of the error-correction pulses to a plurality of sequentially decreasing rates after the charge ~~reaches~~ equals the first threshold.

6. (Currently amended) The phase-lock loop according to Claim 5, wherein the rate selector holds the rate of the error-correction pulses at a predetermined minimum rate once the ~~minimum~~ rate decreases to the minimum rate~~is reached~~.

7. (Currently amended) A phase-lock loop comprising:

an oscillator having an output oscillator signal whose frequency is related to a received error-correction signal:

a phase-frequency circuit receiving the oscillator signal and a reference signal and generating at a controllable rate error-correction pulses based on a phase difference between the oscillator signal and the reference signal;

a filter generating the error-correction signal from the error-correction pulses, the filter including a capacitor;

a rate selector coupled to the capacitor and to the phase-frequency circuit, monitoring a charge on the capacitor, and controlling the rate at which the phase-frequency circuit generates the error-correction pulses as a function of the charge on the capacitor;~~The phase-lock loop according to Claim 1,~~

wherein the phase-detector circuit determines the phase difference between the oscillator and reference signals during comparison cycles;

~~-~~wherein the rate selector includes a counter to count the comparison cycles; and

wherein ~~-~~the rate selector causes the phase-frequency circuit to generate the error-correction pulses at a rate that is related to ~~uses~~ the count of the counter and to the capacitor voltage~~ to set the variable rate~~.

8. (Currently amended) The phase-lock loop according to Claim 7, wherein the rate selector ~~controls~~ uses the count of the counter to cause the phase-frequency circuit to generate ~~set~~ the error-correction pulses at a plurality of sequentially decreasing rates after the charge equals~~reaches~~ a first threshold.

9. (Currently amended) The phase-lock loop according to Claim 8, wherein the rate selector holds the rate of the error-correction pulses at a predetermined minimum rate once the ~~minimum~~ rate decreases to the minimum rate~~is reached~~.

10. (Currently amended) The phase-lock loop according to Claim 7, wherein the counter is a binary counter having more than L stages, where $1/(2^L)$ is ~~the~~a minimum rate of the error-correction pulses; and the rate selector includes a logic circuit using the count of the stages and the voltage on the capacitor to set the rate of the error-correction pulses.

11. (original) The phase-lock loop according to Claim 10, wherein the counter has 2^L stages.

12. (Currently amended) The phase-lock loop according to Claim 11, wherein the logic circuit sequentially decreases the rate of the error-correction pulses to $1/(2^L)$.

13. (Currently amended) The phase-lock loop according to Claim 12, wherein the rate selector holds the rate of the error-correction pulses at the minimum rate once the rate decreases to the minimum rate~~is reached~~.

14. (Currently amended) The phase-lock loop according to Claim 10, wherein the logic circuit use the L and more than L stages until the rate of the error-correction pulses decreases to ~~reaches~~ the minimum rate; and the logic circuit use the L stages to hold the rate at the minimum rate once the rate decreases to the minimum rate~~is reached~~.

15. (Currently amended) The phase-lock loop according to Claim 1, wherein the phase-frequency circuit includes a phase-frequency detector generating the error-correction pulses and includes~~ing~~ a logic circuit between the phase-frequency detector and the filter which transmits the error-correction

pulses to the filter ~~signal through~~ under the control of the rate selector.

16. (original) A pulse width modulation controller including a phase-lock loop according to Claim 1; and wherein the reference signal is a master PWM signal and the oscillator signal is a slave PWM signal of the controller.

17. (Currently amended) A power supply circuit comprising:

a main power supply;

a master PWM power supply that generates a first regulated supply voltage from the main power supply and that generates a master PWM signal; and

a slave PWM power supply that receives the master PWM signal and generates a second regulated supply voltage from the main power supply and includes a phase-lock loop; and

wherein the phase-lock loop is according to Claim 1 and wherein the reference signal is the master PWM signal and the oscillator signal is a slave PWM signal used to regulate the second regulated supply voltage.

18. (Currently amended) A power supply circuit comprising:

a main power supply;

a master PWM power supply that generates a first regulated supply voltage from the main power supply and that generates a master PWM signal; and

a slave PWM power supply that receives the master PWM signal and generates a second regulated supply voltage from the main power supply and includes a phase-lock loop;

wherein the phase-lock loop is according to Claim 1 and wherein the reference signal is the master PWM signal and the oscillator signal is a slave PWM signal used to regulate the second regulated supply voltage; ~~The power supply circuit according to Claim 17,~~

wherein the master PWM power supply includes a soft-start circuit which generates a master disable signal during a predetermined master soft-start period beginning from start-up; and

wherein the slave PWM power supply includes a soft-start circuit which disables outputting of the slave PWM signal for a predetermined slave soft-start period beginning from termination of the master disable signal, and the phase-lock loop operates prior to the termination of master disable signal to lock on the master PWM signal.

19. (original) The power supply circuit according to Claim 18, wherein the master soft-start period is greater than a period of time for the slave's phase-lock loop to achieve lock.

20. (original) A transmitter/receiver comprising:

a receiver circuit which generates a received base-band data signal from a modulated received signal and a local oscillator signal;

a transmitter circuit which generates a modulated transmission signal from a transmission base-band data signal and a local oscillator signal; and

a phase-lock loop coupled to the receiver and transmitter circuits; and

wherein the phase-lock loop is according to Claim 1.

21. (original) A computer system comprising:

a central processing unit connected to a bus system;

a video processor connected to the bus system, controlled by the central processing unit and including a power supply circuit;

a display device connected to the video processor; and

wherein the power supply circuit is according to Claim 17.